WHAT IS CLAIMED IS:

1. A hard macro for use in an Application Specific Integrated Circuit (ASIC), comprising:

an input/output (I/O) port having a port metallic conductor of a low level metalization layer;

an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and

an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor.

2. The hard macro of claim 1, wherein the first and second conducting sections include a plurality of vias extending vertically between adjacent metalization layers.

3. The hard macro of claim 1, wherein the hard macro is selected from a group consisting of a processor, memory, an input interface circuit, an output interface circuit, an encoder, and a decoder.

4. An integrated circuit including a plurality of the hard macros of claim 1.

5. A method of forming a hard macro for use in an Application Specific Integrated Circuit, comprising steps of:

(a) forming a port level conductor of the I/O port in a low level metalization layer;

(b) forming an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

(c) forming a top level metallic conductor in a highest level metalization layer that is electrically coupled to a diffusion region;

(d) forming a first conducting section of an electrical connection extending from the gate conductor to the top level metallic conductor; and

(e) forming a second conducting section extending from the top level metallic conductor to the port level conductor.